VLSI DESIGN OF LOW POWER HIGH SPEED DOMINO LOGIC

Ms. Rakhi R. Agrawal*

Dr. S. A. Ladhake**

Abstract:

Simple to implement, low cost designs in CMOS Domino logic are presented. These designs require less transistors and are full Domino logic compatible while they attain better performance compared to the standard Domino logic implementations. Wide fan-in logic such as domino circuits is used in high-performance applications. Dynamic domino logic circuits are widely used in modern digital VLSI circuits. The novel feature of dynamic circuits is often favoured in high performance designs because of the speed advantage offered over static CMOS logic circuits. This paper compares static CMOS, domino (dynamic) logic design implementations.

Keywords: CMOS, Domino Logic (Dynamic), Power Dissipation, Low Power, High Speed.

* Electronics and Telecommunication, Sipna's college of Engineering and Technology, Amravati, India.

** Principal, Sipna's college of Engineering and Technology, Amravati, India.

Introduction:

Domino logic is the most popular dynamic logic. Owing to its high performance characteristic, Domino logic is widely used in custom circuit design to achieve higher speed, smaller area and potentially lower power consumption due to glitch-free operation. However, Domino logic circuits can implement only non-inverting logic; the synthesis of a Domino logic circuit typically involves the conversion to a unate representation from the original binate logic network. Synthesis of domino circuits is more complicated than that of static circuits. The added complexity is due to domino logic's monotonic nature which forces it to implement only non-inverting functions. Therefore, domino logic can only be mapped to a network of non-inverting functions, where needed logic inversions must be performed at either primary inputs and/or primary outputs. Any random logic network can be transformed into a network of non-inverting functions by finding a unate network representation. There are also difficulties in designing and verifying this class of circuits. Dynamic circuitry can become highly sensitive to clock skew, charge sharing etc. Dynamic domino logic circuits are widely used in modern VLSI circuits. These dynamic circuits are often favoured in high performance designs because of the speed advantage offered over static CMOS logic. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power dissipation. This work discusses domino circuit design techniques to reduce the power dissipation of domino logic while simultaneously improving noise immunity. Domino logic has created a substantial interest due to its performance and CMOS power consumption. It runs 1.5-2 times faster than static CMOS logic because dynamic gates present much lower input capacitance for the same output current and a lower switching threshold.

Domino input signals to domino gates:

A domino input signal to a domino gate must satisfy the following setup and hold timing constraints for correct operation of the gate.

Data input must rise before CLOCK falls, i.e., before the end of evaluate cycle. This setup constraint ensures that domino gate output evaluates before end of the evaluate cycle.

Data input must fall before CLOCK rises, i.e., data input must precharge before beginning of next evaluate cycle. This setup constraint ensures that domino gate output is precharged before the end of precharge cycle.

Data input falling must be held after the dynamic output node falls.

Motivation:

In parallel system speed, power is high and in addition area constraint is also high .To reduce the power and area we prefer domino logic concept. Domino logic has become the logic family of choice for high speed and compact circuits. The reduced input capacitance and use of NMOS logic transistors make domino circuits faster and smaller than their static counterparts. So there is need of such a design which balance the both things from designer side, that is speed , power and area constraints. This is motivation to design a Domino Logic Circuit.

Concept of Domino Logic:

Dynamic logic is over twice as fast as normal logic; it uses only fast N transistors. Static logic is slower because it uses slow P transistors to compute logic. Dynamic logic is harder to work, but if we need the speed there is no other choice. Dynamic logic requires two phases, the first phase is set up phase or pre charge phase, in this phase the output is unconditionally go to high (no matter the values of the inputs A and B).The capacitor which represents the load capacitance of this gate becomes charged. During the evaluation phase, CLK is high. Popular implementation of dynamic logic is domino logic. Domino logic is a CMOS based evaluation of the dynamic logic techniques which are based on the either PMOS or NMOS transistors. It was developed to speed up the circuits. The dynamic gate outputs connect to one inverter, in domino logic. In domino logic, cascade structure consisting of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to “1” (until the next clk cycle), just as dominos, once fallen, cannot stand up. The structure is hence called domino CMOS logic.

Domino logic is the most popular dynamic logic. It runs 1.5-2 times faster than static CMOS logic because dynamic gates present much lower input capacitance for the same output current and a lower switching threshold. Domino circuits are in function very similar to the clocked CMOS circuit. In Domino logic a single clock is used to precharge and evaluate a cascaded set of dynamic logic blocks. This circuitry incorporates a static CMOS buffer into each logic gate as shown in Figure 1. During the precharge phase (CK=0) all output nodes all (N') of the dynamic gates are precharged to high, through the transistor MP, and thus the outputs (N) of the corresponding buffers are precharged to low. Since all transistors of subsequent dynamic gates are fed from such buffers, these will be turned off during the precharge phase.

A domino logic gate precharges when the clock is low and it evaluates when the clock is high, i.e., the output of every domino gate falls (precharges) before the evaluate cycle and it conditionally rises during the evaluate cycle. Thus, for domino input signals to a domino gate, the setup and hold constraints as outlined above are naturally satisfied as long as the cascaded sequence of domino gates can be evaluated within the evaluate clock phase. In contrast, when an unclocked signal such as a static signal is presented as an input to a domino gate, it is nontrivial to satisfy these setup and hold constraints.

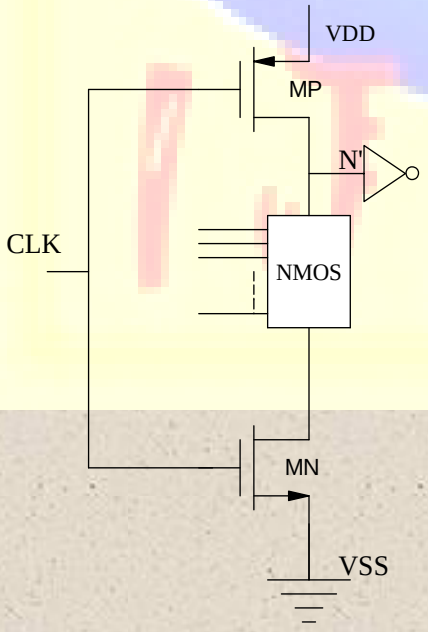

FIGURE 1. A DOMINO LOGIC CIRCUIT.

Next, during the evaluation phase, nodes N' are either discharged through transistor MN or they remain high, according to the realized function. Thus the outputs N of the buffers either go to high or remain low, respectively. It should be noted that in Domino logic the transition of nodes N is always from low to high and it is rippled through the logic from the primary inputs lo the primary outputs. Since there are cascaded logic blocks, the evaluation of a stage causes the next stage to evaluate arid so on. Obviously, any number of logic stages may be cascaded, provided that they can be evaluated within the evaluate phase of the clock. In this paper Domino logic design is used for better performance with a smaller number of transistors. In a novel Domino logic design precharged by clock and data has been proposed that also presents high performance and reduced area requirements.

Sources of Power Dissipation:

The power consumed by CMOS circuits can be classified into two categories:

1. Dynamic Power Dissipation:

For a fraction of an instant during the operation of a circuit, both the PMOS and NMOS devices are "on" simultaneously. The duration of the interval depends on the input and output transition (rise and fall) times. During this time, a path exists between Vdd and Gnd and a short-circuit current flows. However, this is not the dominant factor in dynamic power dissipation. The major component of dynamic power dissipation arises from transient switching behaviour of the nodes. Signals in CMOS devices transition back and forth between the two logic levels, resulting in the charging and discharging of parasitic capacitances in the circuit. Dynamic power dissipation is proportional to the square of the supply voltage. In deep sub-micron processes, supply voltages and threshold voltages for MOS transistors are greatly reduced. This, to an extent, reduces the dynamic power dissipation.

2. Static Power Dissipation:

This is the power dissipation due to leakage currents which flow through a transistor when no transactions occur and the transistor is in a steady state. Leakage power depends on gate length and oxide thickness. It varies exponentially with threshold voltage and other parameters. Reduction of supply voltages and threshold voltages for MOS transistors, which helps to reduce dynamic power dissipation, becomes disadvantageous in this case. The subthreshold leakage current increases exponentially, thereby increasing static power dissipation.

Need of Domino Logic:

Avoids duplicating logic twice as both N-tree and P tree, as in standard CMOS. Typically can be used in very high performance applications. Very simple sequential memory circuits; amenable to synchronous logic. High density achievable. And also try to consumes less power (in some cases).

Conclusion:

We have proposed systematic technique named as Domino Logic circuit. Domino Logic circuit are implemented because it has number of advantages such as smaller area than fully static gates. Also smaller parasitic capacitances hence higher speed. Reliable operation if correctly designed. This makes dynamic logic a good choice for those parts of a circuit. This paper compares static CMOS, domino (dynamic) logic design implementations.

References:

- Chua-Chin Wang, Chi-Chun Huang, Ching-Li Lee, and Tsai-Wen Cheng, " A Low Power High-Speed 8-Bit Pipelining CLA Design Using Dual-Threshold Voltage Domino Logic" ,In *IEEE Transactions on very Large Scale Integration (VLSI) Systems*, Volume 16, No. 5, May 2008.

- Vojin G. Oklobdzija and Robert K. Montoye, "Design-Performance Trade-Offs in CMOS-Domino Logic", In *IEEE Journal of Solid-State Circuits*, Volume sc-21, No. 2,
- Salendra.Govindarajulu1, Dr.T.Jayachandra Prasad, P.Rangappa , "Low Power, Reduced Dynamic Voltage Swing Domino Logic Circuits", *Salendra. Govindarajulu et. al. / Indian Journal of Computer Science and Engineering*, Volume 1 No 2, 74-81
- Salendra.Govindarajulu, Dr.T.Jayachandra Prasad, C.Sreelakshmi, Chandrakala, U.Thirumalesh, "Energy Efficient, Noise-Tolerant CMOS Domino VLSI Circuits in VDSM Technology", *(IJACSA) International Journal of Advanced Computer Science and Applications*, Volume 2, No. 4, 2011.
- Jacobus A. Pretorius and Andre T. Salama, "Latched Domino CMOS Logic", *IEEE Journal of Solid-States Circuits*,Volume SC-21,NO. 4, August 1986
- Shih-Chieh Chang, Ching-Hwa Cheng, Wen-Ben Jone, Shin-De Lee, and Jinn-Shyan Wang, *"*Charge-Sharing Alleviation and Detection for CMOS Domino Circuits*", IEEE Transactionson Computer- Aided Design of Integrated Circuits and Systems* Volume 20, No. 2, Feburay 2001
- Salendra.Govindarajulu, Dr. T.Jayachandra Prasad, "Design of High Performance Dynamic CMOS Circuits in Deep Submicron Technology", Salendra Govindarajulu et. al. / International Journal of Engineering Science and Technology Vol. 2(7), 2010.